AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of the claims, which replaces all prior versions thereof.

Claims 1-16 (cancelled).

17. (Currently Amended) A transistor formed on a substrate assembly, comprising:

a raised drain structure;

a raised source structure;

a gate located between said source and said drain;

a first capping layer in communication with at least a portion of said gate and said source;

a first portion of a gate oxide region in communication with at least a portion of said gate and said source;

a first implant junction area located in said substrate assembly extending partially beneath said gate and said source, wherein said first junction area includes a first pocket implant junction and a first outdiffusion area, wherein said first pocket implant junction is counterdoped by a substrate dopant;

a second capping layer in communication with at least a portion of said gate and said drain;

a second portion of said gate oxide region in communication with at least a portion of said gate and said drain; and

a second implant junction area located in said substrate assembly extending partially beneath said gate and said drain, wherein said second junction area includes a

second pocket implant junction and a second outdiffusion area, wherein said second pocket implant junction is counterdoped by said substrate dopant.

Claim 18 (cancelled).

19. (Original) The transistor of claim 17 wherein said first and second junctions include doped areas.

Claims 20-97 (cancelled).

98. (Previously Presented) The transistor of claim 17, wherein said raised source includes doped polysilicon.

99. (Previously Presented) The transistor of claim 17, wherein said raised drain includes doped polysilicon.

100. (Previously Presented) The transistor of claim 17, wherein said gate includes doped polysilicon.

101. (Previously Presented) The transistor of claim 17, wherein said source includes a plug.

102. (Previously Presented) The transistor of claim 101, wherein said plug includes an adhesive layer.

103. (Previously Presented) The transistor of claim 17, wherein said gate includes a gate terminal.

Claims 104-124 (cancelled).

125. (Currently Amended) A transistor formed on a substrate assembly, comprising:

a raised drain structure;

a raised source structure;

a gate located between said source and said drain;

a first capping layer in communication with at least a portion of said gate and said source;

a first portion of a gate oxide region in communication with at least a portion of said gate and said source;

a first implant junction area located in said substrate assembly extending partially beneath said gate and said source, wherein said first junction area includes a first outdiffusion area and a first pocket implant junction comprising a first doped silicon area, wherein said first doped silicon area is counterdoped by a substrate dopant;

a second capping layer in communication with at least a portion of said gate and said drain;

a second portion of said gate oxide region in communication with at least a portion of said gate and said drain; and

a second implant junction area located in said substrate assembly extending partially beneath said gate and said drain, wherein said second junction area includes a

second outdiffusion area and a second pocket implant junction comprising a second doped silicon area, wherein said second doped silicon area is counterdoped by said substrate dopant;

126. (Previously Presented) The transistor of claim 125, wherein said doped silicon areas include phosphorous.

Claim 127 (cancelled).

128. (Currently Amended) A transistor formed on a substrate assembly, comprising:

a raised drain structure;

a raised source structure;

a gate located between said source and said drain;

a first capping layer in communication with at least a portion of said gate and said source;

a first portion of a gate oxide region in communication with at least a portion of said gate and said source;

a first implant junction area located in said substrate assembly extending partially beneath said gate and said source, wherein said first junction area includes a first pocket implant junction and a first outdiffusion area, wherein said first pocket implant junction is counterdoped by a substrate dopant;

a second capping layer in communication with at least a portion of said gate and said drain;

a second portion of said gate oxide region in communication with at least a portion of said gate and said drain; and

a second implant junction area located in said substrate assembly extending partially beneath said gate and said drain, wherein said second junction area includes a second pocket implant junction and a second outdiffusion area, wherein said second pocket implant junction is counterdoped by said substrate dopant.